

## SIMULINK MODEL OF DIODE-CLAMPED MULTILEVEL INVERTERS

Adrian ŞCHIOP

Department of Electronics, University of Oradea, Romania, [aschiop@uoradea.ro](mailto:aschiop@uoradea.ro)

**Abstract:** This paper presents a contribution to modelling of the diode-clamped multilevel inverter. The models presented are used to perform a harmonic analysis of the output voltage of the multilevel inverters. The command method used in this work is based on the sinusoidal PWM. The simulation results were obtained for different operation modes due to the sinusoidal PWM modulation. This type of model can be used then to the design of these inverters but also in the didactic activities of the students from electrical and electronic engineering specializations

**Keywords:** diode clamped multilevel inverter, modelling, Simulink, harmonic analysis

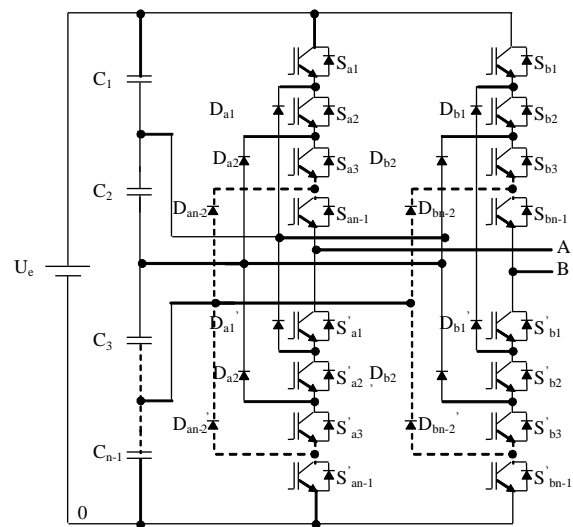
### 1. INTRODUCTION

Nowadays, the multilevel inverters are used more and more in different applications. The main advantage of a multilevel inverter is the higher quality of its output voltage. During the time were developed many kind of multilevel inverters. This fact demonstrates once again the importance of these converters. From their advantages one can mention: the low value of the voltage on each power semiconductor switches [1], a low total harmonic distortion of the output voltage and power quality. A survey of the main topologies of multilevel inverters is presented in [2], [3]. In this paper is presented a new model for a diode-clamped multilevel inverter. This model can be used for design or study. The simulation results were accomplished by the Simulink platform and those shown different operation modes for 3, 4 and 5 diode-clamped multilevel inverters. This article offers a new model useful for the investigation of the performances of multilevel converter with clamped diodes tacking into account the number of the level and the spectrum of the output voltage. This model was used for the sinusoidal PWM control. The simulation results are in good agreement with other similar valuable results obtained by other researchers.

### 2. BRIEF DESCRIPTION OF THE DIODE - CLAMPED MULTILEVEL INVERTER

The circuit diagram of an “n”-level inverter is shown in the next figure. The inverter

contains n-1 capacitors that will assure between point A or B and the ground an output voltage with n levels.



**Fig.1. Circuit diagram for a multilevel inverter**

The maximum voltage on each power semiconductor switch is limited to the  $U_e/(n-1)$ , where  $U_e$  is the input voltage of the inverter. The higher the number of the switches on an inverter leg the smaller the voltage on each switch. The clamping diodes  $D_{xk}$  on upper leg must support different reverse voltage values tacking into account the next relation:

$$u_{D_{xk}} = k \frac{U_e}{n-1} \quad (1)$$

where x represent the leg “a” or “b” of the

inverter and  $k = 1, \dots, (n-2)$ .

To solve this problem it is possible to connect in series diodes with the same characteristics. The clamping diodes  $D_{xk}$  on the lower leg support a voltage with the next values:

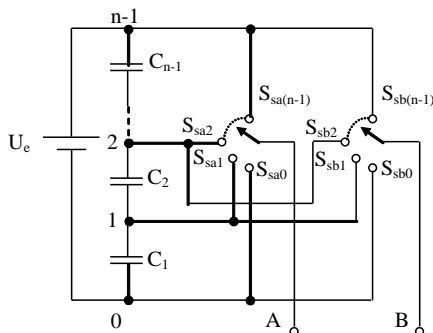
$$u_{D'_{xk}} = (n - 1 - k) \frac{U_e}{n - 1} \quad (2)$$

where  $x$  represents the leg “a” or “b” of the inverter and  $k = 1, \dots, (n-2)$ .

This topology assures a small number of capacitors and the inverter is connected to a single power supply. To use a small number of reactive components is an advantage of this topology. The command method used for this inverter is based on sinusoidal PWM (SPWM). It is possible then to control the RMS value and the frequency of the output voltage.

### 3. MODELLING OF THE DIODE-CLAMPED MULTILEVEL INVERTER

In this work, it is proposed a functional model for the general case of a diode-clamped multilevel inverter. The model is achieved by the help of a switch with “ $n$ ” positions. For the multilevel inverter depicted in figure 1, the two switches  $S_{xi}$  and  $S'_{xi}$  are complementary commanded. Tacking into account this detail, the inverter shown in figure 1 can be modeled by the help of the “ $n$ ” positions switches system.



**Fig.2. Equivalent model of the diode-clamped multilevel inverter based on “ $n$ ” position switches**

For each equivalent switch of the inverter  $S_{sx}$  with  $x = \{a, b\}$  are defined the commutation functions  $s_{sxj} \in \{0,1\}$  with  $j = 0, 1, \dots, (n-1)$ .  $s_{sxj} = 1$  when the output  $X = \{A, B\}$  is connected at the position “ $j$ ” of the

switch  $S_{sx}$ . The time variation of the commutation function depends on the modulation technique for control. In this study was used the SPWM modulation. For each equivalent switch is valid the next relation:

$$\sum_{j=0}^{n-1} s_{sxj} = 1 \quad (3)$$

where  $x = \{a, b\}$ . The value of the voltage  $u_{x0}$  between the points  $x$  and the ground as a function of the voltage  $u_{cp}$  on each capacitor is:

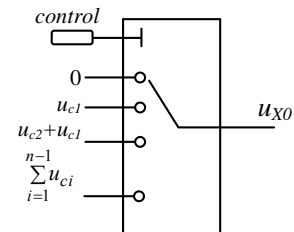
$$u_{x0} = \sum_{j=1}^{n-1} \left( s_{sxj} \sum_{p=1}^j u_{cp} \right) \quad (4)$$

where  $x = \{a, b\}$  and  $X = \{A,B\}$ . When the voltages on each capacitor are equal then (4) become:

$$u_{x0} = \frac{U_e}{n-1} \sum_{j=1}^{n-1} j s_{sxj} \quad (5)$$

where  $x = \{a, b\}$  and  $X = \{A,B\}$ .

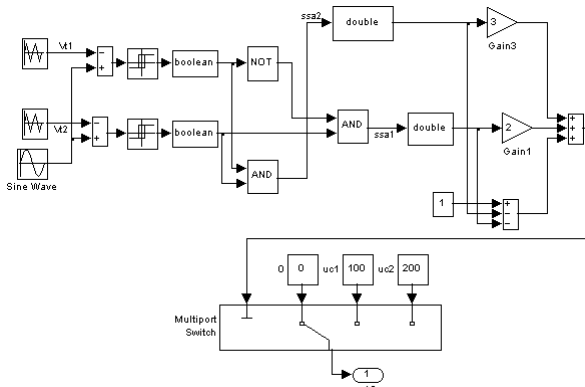
In the general case, the commutation function  $s_{sxj}$  command  $(n-1)$  switches from a leg of the inverter. In figure 3 it is presented the implementation of the proposed model using a multiport switch from Simulink. At the output of the multiport switch is obtained the desired voltage level mentioned in the relations (4) and (5).



**Fig.3. Simulink – Multiport switch**

### 4. SIMULATION OF THE MULTILEVEL INVERTERS OPERATION

Using the proposed model and Simulink platform one can see in figure 4 the circuit diagram developed for the simulation of the inverters operation. In this figure one can see the presence of a multiport switch set for a 3-level inverter. The circuit offers the output voltage for a single leg.

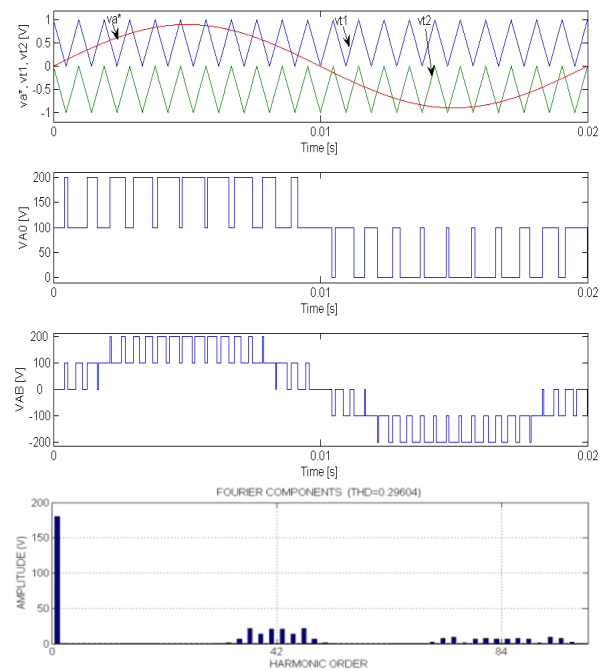


**Fig.4. Simulink model for phase voltage for 3-level inverters**

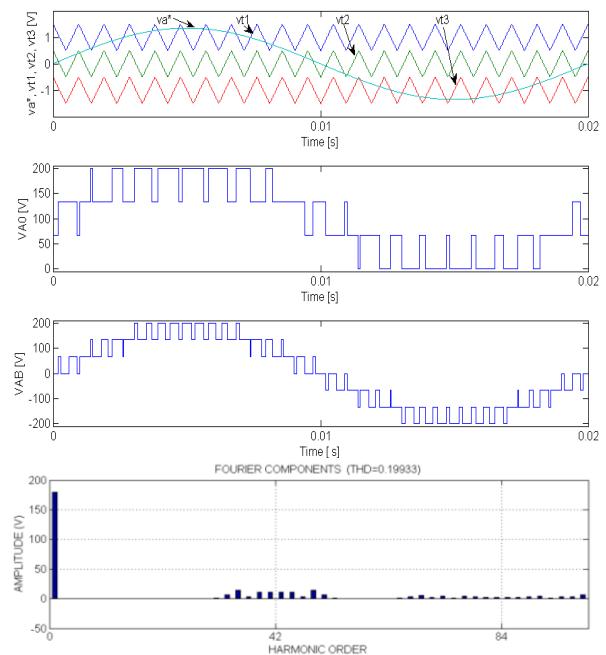
The modulation technique used for these simulations is sinusoidal PWM (SPWM). The SPWM modulation can be accomplished for each phase in two manners: by the help of (n-1) triangular carrier signals overlapped covering a continuous domain and a sinusoidal modulator signal (operation mode A) or by (n-1) triangular carrier signals with a  $T/(n-1)$  phase shift between them and a sinusoidal modulator signal (operation mode B). For the operation mode A there are another three operation sub-modes that depends on the phase shift between the carrier signals: A1 when the triangular carrier signals are in phase, A2 when the carriers signals are alternately  $180^\circ$  phase shifted between them and A3 when an  $180^\circ$  phase shift is encountered between the positive and negative carrier signals. A3 operation mode can be used only for the inverters with odd levels of the output voltages. In the case of the 3-level inverters the modes A2 and A3 are similar [4].

The operating mode A1 is presented in Fig. 5 for three level inverter, in Fig. 6 for four level inverter and in Fig 7 for five level inverter. A2 mode is presented in Fig. 8 for three level inverter, in Fig. 9 for four level inverter and in Fig 10 for five level inverter. A3 mode is presented in Fig.11 for five level inverter.

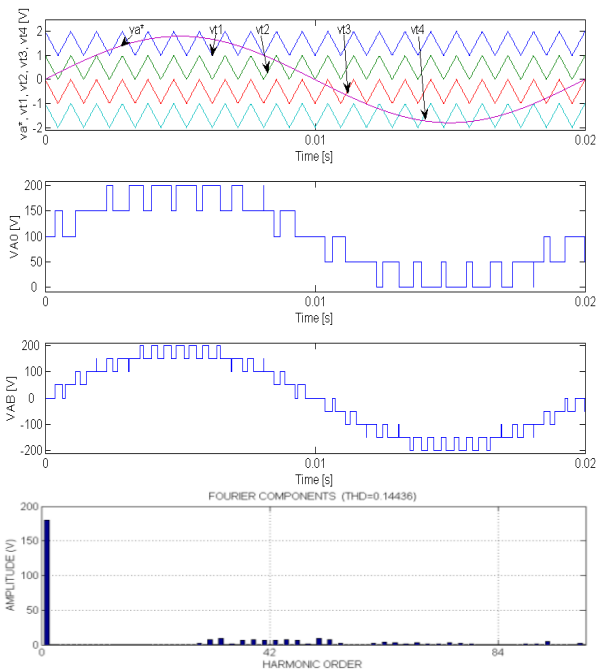
All the simulations for operation modes A1, A2, A3, used the next parameters: input voltage  $U_e = 200V$ , amplitude modulation index is set to 0.9, frequency modulation index is set to the 21, the frequency of the carrier signals is 1050 Hz and the frequency of the modulator signal is 50 Hz [5], [6].



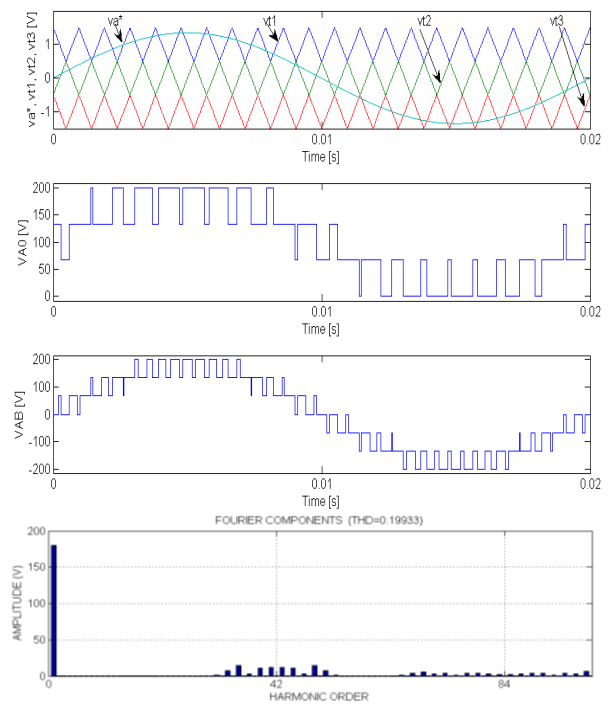
**Fig.5. Sinusoidal modulation, operation mode A1, for 3-level bridge inverter. a) two triangle carriers and sinusoidal modulator signal, b) phase voltage, c) output voltage, d) spectrum of the output voltage.**



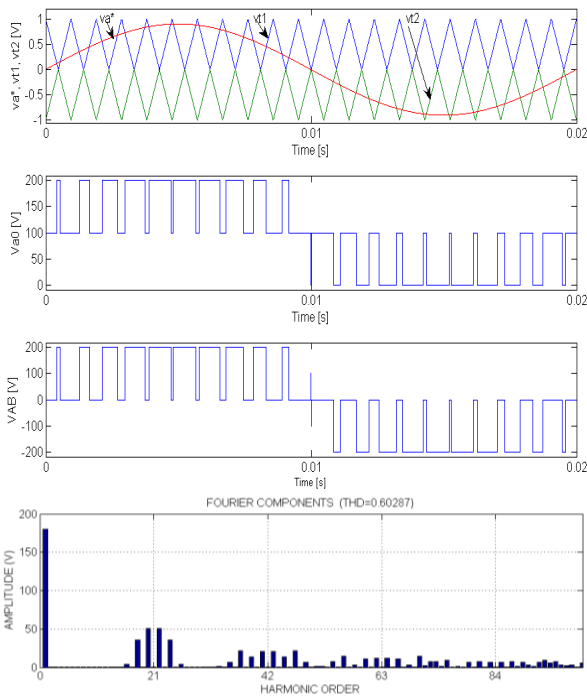
**Fig.6. Sinusoidal modulation, operation mode A1, for 4-level bridge inverter. a) three triangle carriers and sinusoidal modulator signal, b) phase voltage, c) output voltage, d) spectrum of the output voltage.**



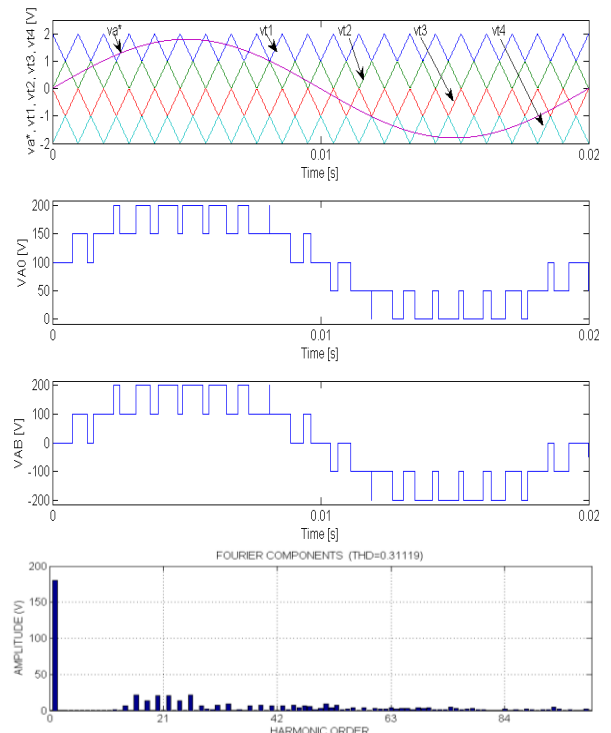
**Fig.7. Sinusoidal modulation, operation mode A1, for 5-level bridge inverter. a) four triangle carriers and sinusoidal modulator signal, b) phase voltage, c) output voltage, d) spectrum of the output voltage.**



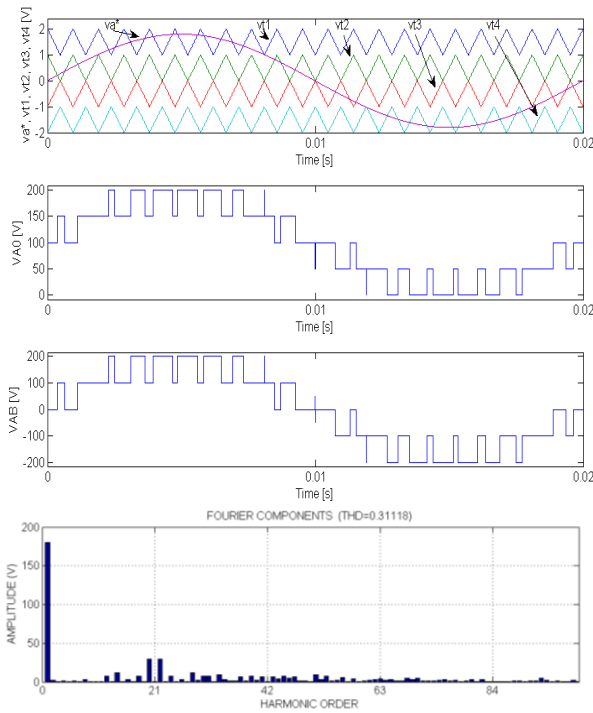
**Fig.9. Sinusoidal modulation, operation mode A2, for 4-level bridge inverter. a) two triangle carriers and sinusoidal modulator signal, b) phase voltage, c) output voltage, d) spectrum of the output voltage.**



**Fig.8. Sinusoidal modulation, operation mode A2, for bridge 3-level inverter. a) two triangle carriers and sinusoidal modulator signal, b) phase voltage, c) output voltage, d) spectrum of the output voltage.**

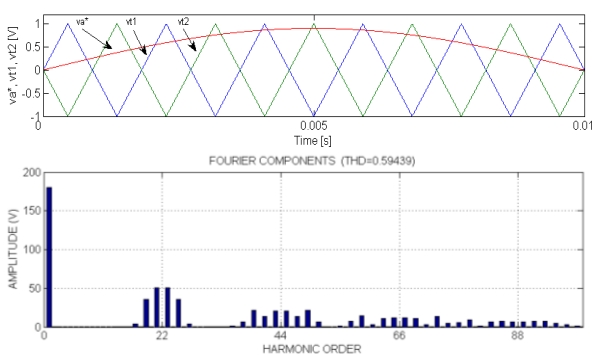


**Fig.10. Sinusoidal modulation, operation mode A2, for 5-level bridge inverter. a) four triangle carriers and sinusoidal modulator signal, b) phase voltage, c) output voltage, d) spectrum of the output voltage.**

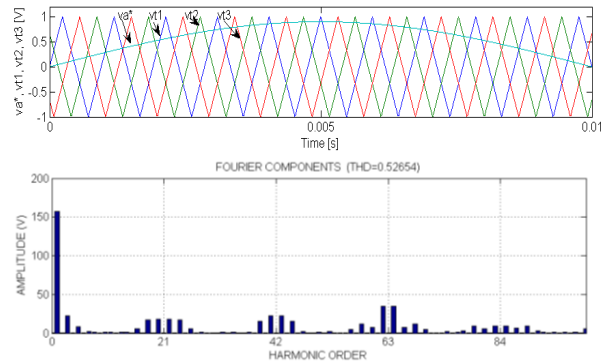


**Fig.11. Sinusoidal modulation, operation mode A3, for 5-level bridge inverter. a) four triangle carriers and sinusoidal modulator signal, b) phase voltage, c) output voltage, d) spectrum of the output voltage.**

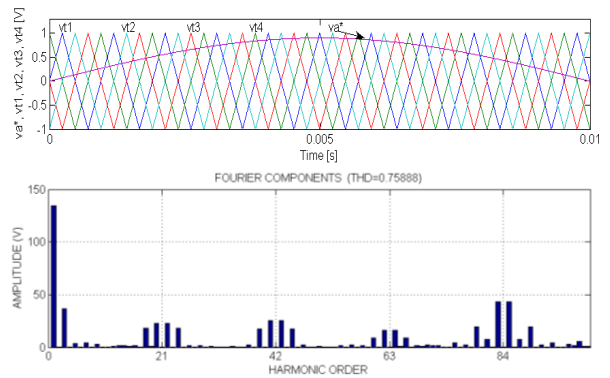
These parameters were kept for the operation mode B. For the operation mode B the carrier signals are phase shifted with  $T_p/(n-1)$ , where  $T_p$  represents the period of the carrier signals and  $n$  represents the level number of the inverter. The inverter controlled by the help of this operation mode generates low order odd harmonics.



**Fig.12. Sinusoidal modulation, operation mode B, for 3-level bridge inverter. a) two triangle carriers and sinusoidal modulator signal, b) spectrum of the output voltage.**



**Fig.13. Sinusoidal modulation, operation mode B, for 4-level bridge inverter. a) three triangle carriers and sinusoidal modulator signal, b) spectrum of the output voltage.**



**Fig.14. Sinusoidal modulation, operation mode B, for 5-level bridge inverter. a) four triangle carriers and sinusoidal modulator signal, b) spectrum of the output voltage.**

The results obtained by simulation are used to determine the values of THD for different placement of the carrier signals as one can see in the table 1.

**Tab.1. THD for output voltage of diode-clamped multilevel inverter.**

Operation mode	THD		
	3-level inverter	4-level inverter	5-level inverter
A1	0.296	0.199	0.144
A2	0.602	0.199	0.311
A3	0.602	-	0,311
B	0.594	0.526	0.758

Using the operation mode A2 produces THD values greater than operation mode A1 for odd level bridge inverters. The value of the THD is the same for the even level bridge inverter when they operate in A1 and A2

modes. For A2 operation mode the harmonics of the output voltage for odd level bridge inverters are concentrated around the switching frequency multiples. For A1 operation mode the harmonics of the output voltages for even level bridge inverters are concentrated next to the double switching frequency multiples. The output voltage of the inverters controlled by operation mode B presents a purely THD for all multilevel inverters. The best result was obtained using the operation mode A1 at the 5-level bridge inverters.

## 5. CONCLUSIONS

Tacking into consideration the model that was presented in this work, it was possible to determine the total harmonic distortion of the output voltage for the 3 -, 4 -, 5 -level diode-clamped inverter. The simulations were accomplished by the help of the Simulink platform.

The main results of the simulations are as follow: for the A1 operation mode the harmonics are grouped around the double switching frequency multiples; for the A2 operation mode of the odd level inverters, the harmonics are grouped around the multiples of the switching frequency and for the even level inverters, the generated harmonics are grouped around the double switching frequency multiples; in the case of the A3 operation mode, the generated harmonics

are concentrated around the switching frequency multiples; the B operation mode determine the presence of the odd harmonics of low order. The simulation results are in good agreement with those of similar studies.

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